Attorney's Docket No.: 42390.P7178 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Horigan, et al. Application No. 09/470,092 Filed: 12/21/1999 For: METHOD AND APPARATUS FOR ENCODING INFORMATION IN AN IC PACKAGE	Examiner: Matthew E. Warren Art Unit: 2815 **FIRST CLASS CERTIFICATE OF MAILING** I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Mail Stop Appeal Briefs - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, V.A. 22313-1450 on 06/07/04 Judy L. Steinkraus Date

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APPEAL BRIEF UNDER 37 C.F.R. §1.192

Sir:

The Applicant hereby submits this Brief in support of its appeal from a final decision of the Examiner in the above-captioned case.

(1) REAL PARTY IN INTEREST

Intel Corporation of Santa Clara, CA.

(2) RELATED APPEALS AND INTERFERENCES

No related applications.

(3) STATUS OF CLAIMS

In this application, Claim(s) 1-14 are pending.

Claims 1, 2, 7, and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,429,387 (hereinafter "Kuribayashi") in view of U.S. Patent 4,471,408 (hereinafter "Martinez").

Claims 3-6 and 9-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,429,387 (hereinafter "Kuribayashi") in view of U.S. Patent 4,471,408 (hereinafter "Martinez") as applied to claims 1, 2, and 8 above, and further in view of U.S. Patent 6,150,724 (hereinafter "Wenzel").

Applicant appeals the Examiner's decision on Claim(s) 1-14 with respect to the rejection under Sections 103.

(4) STATUS OF AMENDMENTS

A final office action was mailed October 7, 2003 rejecting claims 1-14 for the reasons specified above. No response after final was filed.

The claims found in the Appendix of this Appeal Brief reflect the claims as they are understood by the Applicant to stand at the date of this appeal.

(5) SUMMARY OF INVENTION

The invention generally relates to the field of computer systems, and more specifically, to an integrated (IC) package, such as a BGA package, that provides configuration information to the system.

With reference to the claims at issue, in accordance with one embodiment of the present invention includes an IC package having a substrate, a ground

line, and an encoded region. The encoded region provides information based upon selective deposition of solder balls electrically coupled to the ground lines. This information may indicate, for example, a voltage supply level for the processor. (See pages 4-6, and Figure 1A).

6) ISSUES

In the Final Office Action mailed October 7, 2003, the Examiner has:

(1) continued a rejection under Section 103 of Claim(s) of claims 1, 2, 7, and 8 based on Kuribayashi in view of Martinez.

The question presented on this Appeal is:

(1) Whether the combination of Kuribayashi and Martinez renders the claimed invention obvious?

(7) GROUPING OF CLAIMS

Claims 1-14 are grouped together.

(8) ARGUMENT

Question 1 -- Whether the combination of Kuribayashi and Martinez renders the claimed invention obvious?

THE PRESENT INVENTION IS PATENTABLE OVER KURIBAYASHI IN VIEW OF MARTINEZ BECAUSE THERE IS NO REASONABLE EXPECTATION OF COMBINING THE REFERENCES

Applicant respectfully submit that Kuribayashi and Martinez fail to teach or suggest Applicants' invention as claimed, including, for example, Applicants' claimed limitation of "an integrated circuit (IC) package comprising...an

encoded region to provide information based upon selective deposition of solder balls electrically coupled to the ground line" as set forth in claim 1. A similar limitation is also set forth in independent claim 8.

It is stated in the outstanding office action that Martinez discloses an integrated circuit in which pins are selectively bent or broken to encode information. A careful reading of Martinez reveals, however, that the pins selectively bent or broken in Martinez are not the pins of the integrated circuit package but rather the pins of a separate *piggyback* device that is clipped to the top of the package. Kuribayashi discloses a BGA package including solder balls formed directly in the underside of the integrated circuit package. Applicants respectfully submit, therefore, that Kuribayashi may not be combined with Martinez in the manner suggested in the manner suggested in the outstanding office action.

Moreover, Applicants respectfully submit that even if combined, these references do not teach or suggest Applicants' invention, as set forth in independent claims 1 and 8, because, for example, there is no teaching or suggestion of how one skilled in the art would attach the piggyback device of Martinez to the surface of the BGA package of Kuribayashi with any reasonable expectation of making top to the solder balls on underside of the BGA package. One skilled in the art would further recognize that such a piggyback device, if extended to the underside of the BGA package, would likely interfere with the electrical coupling between the BGA device and the substrate to which it is soldered (item 50 in Figure 6 of Kuribayashi).

Therefore, Applicants respectfully submit that the combination of Kuribayashi and Martinez do not teach or suggest Applicants' invention as set forth in independent claims 1 and 8, upon which claims 2-7 and 9-14 are dependent.

Applicant respectfully submits, therefore, that Kuribayashi may not be combined with Martinez in the manner suggested in the recent office action, because there would have been no reasonable expectation of successfully modifying Martinez and Kuribayashi at the time Martinez or Kuribayashi was invented. (See Manual of Patent Examining Procedure ¶ 2143.02; See also *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976), and *Ex parte Erlich*, 3 USPQ2d 1011 (Bd. Pat. App. & Inter. 1986).

CONCLUSION

For all of the foregoing reasons, this Board is respectfully requested to remand this application to the Examiner for reconsideration consistent with an order that the Examiner pass this case to issuance unless a proper rejection to the claims can be made.

FEE FOR FILING A BRIEF IN SUPPORT OF APPEAL

Enclosed is a check in the amount of $330.00 to cover the fee for filing of a brief in support of an appeal required under 37 C.F.R. 1.17(f) and 1.192.

CHARGE OUR DEPOSIT ACCOUNT

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: 6/7 2004

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Appendix A

1. (Original) An integrated circuit (IC) package comprising:

a substrate including an IC;

a ground line; and

an encoded region to provide information based upon selective deposition of solder balls electrically coupled to the ground line.

2. (Original) The package of claim 1, wherein the substrate is the substrate of a ball grid array (BGA) package.

3. (Original) The package of claim 2, wherein the IC is a processor.

4. (Original) The package of claim 3, wherein a deposited solder ball in a solder ball area of the encoded region is used to denote a logical "0", and an absence of a solder ball in the solder ball area is used to denote a logical "1".

5. (Original) The package of claim 4, wherein the encoded region includes at least three solder ball areas.

6. (Original) The package of claim 5, wherein the information indicates a voltage supply level for the IC.

7. (Original) The package of claim 1, wherein the information indicates a voltage supply level for the IC.

8. (Original) An electronic component comprising:

a ball grid array (BGA) package including an encoded region to provide information based upon selective deposition of solder balls; and

a printed circuit board (PCB) coupled to the package.

9. (Original) The component of claim 8, wherein the BGA package contains a processor.

10. (Original) The package of claim 9, wherein a deposited solder ball in a solder ball area of the encoded region is used to denote a logical "0", and an absence of a solder ball in the solder ball area is used to denote a logical "1".

11. (Original) The package of claim 8, wherein any deposited solder ball in a solder ball area of the encoded region is electrically coupled to a first node of a resistor on the PCB, and a second node of the resistor is electrically coupled to a power trace on the PCB.

12. (Original) The package of claim 11, wherein the first node is approximately ground if a solder ball is deposited in the solder ball area, and the first node is approximately Vcc if a solder ball is absent from the solder ball area.

13. (Original) The package of claim 12, wherein the encoded region includes at least three solder ball areas.

14. (Original) The package of claim 13, wherein the information indicates a voltage supply level for a processor within the BGA package.